

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-13. (Canceled)

14. (Original) A method for manufacturing a thin film transistor comprising:
forming a lamination layer by laminating a first conductive film, a first insulating film, a second conductive film over an insulating surface in sequence;
etching the laminating layer; and
laminating a semiconductor film, a second insulating film, and a third conductive film over a side surface of the lamination layer in sequence so as to form a gate insulating film and a gate electrode.

15. (Original) A method according to claim 14, wherein etching is performed so that the side surface of the lamination layer is slanted to the insulating surface.

16. (Original) A method for manufacturing a thin film transistor comprising:
forming a first conductive film over an insulating surface;
etching the first conductive film into a desired shape so as to form a first electrode;
forming a first insulating film over the first electrode and the insulating surface;
forming a second conductive film over the first insulating film;
exposing a side surface of the first electrode, the first insulating film, and the second electrode by etching the second conductive film and the first insulating film into

a desired shape so as to form a second electrode;
forming a semiconductor film over the exposed side surface;
etching the semiconductor film into a desired shape;
forming a second insulating film and a third conductive film over the semiconductor film in sequence;
etching the third conductive film into a desired shape so as to form a gate electrode.

17. (Original) A method according to claim 16, wherein the exposed side surface is etched so as to be slanted to the insulating surface.

18. (Currently Amended) A method for manufacturing a thin film transistor comprising:

forming a first conductive film over an insulating surface;
etching the first conductive film so as to form a first electrode;
forming a first insulating film over the first electrode and the insulating surface[[,]];
etching the first insulating film so as to expose a part of the first electrode;
forming a second conductive film over the first insulating film and the first electrode;

etching the second conductive film so as to expose a part of the first electrode and a part the first insulating film, and forming a second electrode;

forming a semiconductor film over the exposed surface of the first electrode, the exposed surface of the first insulating film, and [[the]] a part of the second electrode;

etching the semiconductor film into a desired shape;

forming a second insulating film and a third conductive film over the semiconductor film in sequence; and

etching the third conductive film into a desired shape so as to form a gate electrode.

19. (Original) A method according to claim 18, wherein the exposed surface is etched so as to be slanted to the insulating surface.

20. (New) A method for manufacturing a thin film transistor comprising:
forming a first conductive film over an insulating surface;
forming a first electrode by etching the first conductive film;
forming a first insulating film over the first electrode and the insulating surface;
forming a second conductive film over the first insulating film;
forming a second electrode by etching the first insulating film and the second conductive film, thereby exposing a side surface of the first electrode, the first insulating film, and the second electrode;
forming a semiconductor film over the exposed side surface;
etching the semiconductor film into a desired shape;
forming a second insulating film and a third conductive film over the semiconductor film in sequence; and
forming a gate electrode by etching the third conductive film,
wherein at least one of the first, second, and third conductive film is formed by ink-jet print.

21. (New) A method according to claim 20, wherein the exposed side surface is etched so as to be slanted to the insulating surface.

22. (New) A method for manufacturing a thin film transistor comprising:

forming a first conductive film over an insulating surface;
forming a first electrode by etching the first conductive film;
forming a first insulating film over the first electrode and the insulating surface;
forming a second conductive film over the first insulating film;
forming a second electrode by etching the first insulating film and the second conductive film, thereby exposing a side surface of the first electrode, the first insulating film, and the second electrode;
forming a semiconductor film over the exposed side surface;
etching the semiconductor film into a desired shape;
forming a second insulating film and a third conductive film over the semiconductor film in sequence;
forming a gate electrode by etching the third conductive film;
forming an interlayer insulating film over the second insulating film and the gate electrode; and
forming a wiring over the interlayer insulating film,
wherein the wiring is electrically connected to the second electrode.

23. (New) A method according to claim 22, wherein the exposed side surface is etched so as to be slanted to the insulating surface.

24. (New) A method for manufacturing a thin film transistor comprising:
forming a first conductive film over an insulating surface;
forming a first electrode by etching the first conductive film;
forming a first insulating film over the first electrode and the insulating surface;
forming a second conductive film over the first insulating film;
forming a second electrode by etching the first insulating film and the second

conductive film, thereby exposing a side surface of the first electrode, the first insulating film, and the second electrode;

forming a semiconductor film over the exposed side surface;

etching the semiconductor film into a desired shape;

forming a second insulating film and a third conductive film over the semiconductor film in sequence;

forming a gate electrode by etching the third conductive film;

forming an interlayer insulating film over the second insulating film and the gate electrode; and

forming a wiring over the interlayer insulating film,

wherein the wiring is electrically connected to the first electrode.

25. (New) A method according to claim 24, wherein the exposed side surface is etched so as to be slanted to the insulating surface.